Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (currently amended) A method for fabricating a planar inductor in high-performance high-frequency semiconductor circuits, comprising the steps of:

providing a substrate having a top side and a bottom side wherein said top side has a ~~first~~ passive surface and an active ~~second~~ surface~~,~~ wherein active devices with conductive interconnects ~~being covered by a layer of passivation having been~~ are created over ~~the~~ said active surface of said substrate;

creating at least one pair of planar inductors overlying said passive surface of said substrate;

providing a passivation layer over said passive surface and said active surface of said substrate and overlying said at least one pair of planar inductors;

forming a scribe line penetrating through said passivation layer overlying said passive surface to said passive surface and separating said at least one pair of planar inductors;

attaching a glass panel to ~~the surface of~~ said layer of passivation;

cutting ~~the first surface of~~ said substrate from said bottom side, said cutting being aligned with ~~a~~ said passive ~~region in said second~~ surface of said substrate, said cutting not completely penetrating through said substrate;

thereafter removing from said bottom side all of said substrate material underlying ~~from a~~ said passive ~~region in the second~~ surface of said substrate, exposing at least one first bond pad created on said passive ~~the~~ surface ~~of said passive region~~ on each side of said scribe line; and

cutting said glass panel in alignment with said scribe line.

2. (currently amended) The method of claim 1~~, said substrate~~ further comprising:

~~a first and a second surface, active devices having been created in or on active surface regions in the second surface of said substrate, said active surface regions being separated by a passive surface region, a scribe line having been provided across said passive surface region,~~

providing a layer of insulation ~~having been provided~~ over ~~the surface of~~ said active surfaces;~~regions, at least one bond pad having been provided in said passive surface region on each side of said scribe line~~,

depositing a layer of dielectric ~~having been deposited~~ over ~~the surface of~~ said layers of insulation and over said passive surface; and ~~region separated by said scribe line,~~

forming at least a second ~~one~~ bond pad ~~having been created on the~~ within a top surface of said layer of dielectric on each side of said scribe line~~;~~.

~~creating at least one planar inductor on the surface of said layer of dielectric on each side of said scribe line, said at least one planar inductor overlying said passive surface region of said substrate;~~

~~depositing a layer of passivation over the surface of said layer of dielectric separated by said scribe line;~~

3. (currently amended) The method of claim 2 wherein at least one layer of interconnect lines is provided in said layer of dielectric, said interconnect lines making electrical contact with said active devices provided ~~in on the~~ said active ~~regions~~surface of said substrate, said interconnect lines further being in contact with said ~~at least one~~ first bond pads provided on ~~the surface of~~ said passive ~~region~~surface of said substrate and with said ~~at least one~~ second bond pads provided on ~~the~~said top surface of said layer of dielectric.

4. (currently amended) The method of claim 2 wherein said at least one inductor ~~created on the surface of said layer of dielectric~~ on each side of said scribe line is connected to said at least one second bond pad provided on ~~the~~said top surface of said layer of dielectric on each side of said scribe line.

5-16.(canceled)

17. (new) A method for fabricating a planar inductor in a semiconductor circuit comprising:

providing a substrate having a top side and a bottom side wherein said substrate contains active regions separated by a passive region wherein active devices are formed over an insulating layer in said active regions, wherein at least one pair of first bond pads is formed on said substrate surface in said passive region, wherein a dielectric layer is formed overlying said active devices in said active regions and overlying said at least one pair of first bond pads in said passive region, wherein at least one pair of second bond pads is formed in a top portion of said dielectric layer in said passive region, wherein a passivation layer is formed overlying said dielectric layer, and wherein a scribe line is formed through said passivation layer and said dielectric layer to said substrate in said

passive region wherein said scribe line separates each of said pairs of first bond pads and second bond pads;

attaching a glass panel to said passivation layer;

cutting said substrate from said bottom side in alignment with said scribe line wherein said cutting does not penetrate said substrate to said scribe line;

thereafter removing all of said substrate from said bottom side in said passive region thereby exposing said at least one pair of first bond pads from said bottom side; and

thereafter dicing said substrate along said scribe line.

18. (new) The method according to Claim 17 further comprising

forming at least one pair of planar inductors overlying said dielectric layer in said passive region wherein said passivation layer covers said inductors and wherein said scribe line separates said at least one pair of inductors.

19. (new) The method according to Claim 17 wherein at least one layer of interconnect lines is provided in said dielectric layer, wherein said interconnect lines make electrical contact with said active devices, and wherein said interconnect lines are further in contact with said at least one pair of first bond pads with said at least one pair of second bond pads.

20. (new) The method according to Claim 18 wherein each of said inductors is connected to one of said second bond pads.

21. (new) A method for fabricating a planar inductor in a semiconductor circuit comprising:

providing a substrate having a top side and a bottom side wherein said substrate contains active regions separated by a passive region wherein active devices are formed over an insulating layer in said active regions, wherein at least one pair of first bond pads is formed on said substrate surface in said passive region, wherein a dielectric layer is formed overlying said active devices in said active regions and overlying said at least one pair of first bond pads in said passive region, wherein at least one pair of second bond pads is formed in a top portion of said dielectric layer in said passive region, wherein at least one pair of planar inductors are formed overlying said dielectric layer in said passive region, wherein a passivation layer is formed overlying said dielectric layer, and wherein a scribe line is formed through said passivation layer and said dielectric layer to said substrate in said passive region wherein said scribe line separates each of said pairs of first bond pads, second bond pads, and inductors;

attaching a glass panel to said passivation layer;

cutting said substrate from said bottom side in alignment with said scribe line wherein said cutting does not penetrate said substrate to said scribe line;

thereafter removing all of said substrate from said bottom side in said passive region thereby exposing said at least one pair of first bond pads from said bottom side; and

thereafter dicing said substrate along said scribe line.

22. (new) The method according to Claim 21 wherein at least one layer of interconnect lines is provided in said dielectric layer, wherein said interconnect lines make electrical contact with said active devices, and wherein said interconnect lines are further in contact with said at least one pair of first bond pads with said at least one pair of second bond pads.

23. (new) The method according to Claim 21 wherein each of said inductors is connected to one of said second bond pads.